A HIGH-PERFORMANCE MPEG4 BITSTREAM PROCESSING CORE
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ABSTRACT
Entropy coding is one of the main techniques for lossless data compression in many multimedia applications. In video and image coding standards such as JPEG, MPEG1/2/4, and H.26x, the most often used entropy coding techniques include run-length coding and variable-length coding. Due to the demand of high quality video compression like DTV or HDTV, the complexity of entropy coding increases significantly. This fact motivates the design of high performance entropy decoder proposed in this paper. The proposed IP core exploits the concurrent operations in the MPEG4 entropy decoding to achieve high performance in terms of limited hardware cost. The implementation results show that the proposed IP core operates at 125MHz clock frequency (i.e. 2000 Mbps) with the cost of 0.22 mm² silicon area based on a 0.25um CMOS technology.

1. INTRODUCTION
Variable Length Coding is a widely used lossless data compression technique that has been often found at many image and video coding systems. Besides, it is often applied together with other lossy image compression techniques to further increase the data compression rate. The main idea for variable length coding is to minimize the average codeword length. Shorter codewords are assigned to frequently occurring data and longer codewords are assigned to infrequently occurring data. In MPEG4 video coding standard, most of the coding information is encoded as variable length coded bitstream. Therefore, it is necessary to decode VLC codes fast enough for meeting the real-time demands of high quality video coding systems like DTV or HDTV. Besides, the bitstream parser is another important component in the MPEG4 video decoding system. It splits the bitstream into texture bitstream (usually coded in VLC) and header information (usually coded in fixed length codes denoted as FLCs). Then the decoded information is sent to the right components like texture decoder and motion compensation unit in the MPEG4 video decoding system shown in Fig. 1.

From Fig. 1, the bitstream parser and VLD unit are the main components involving the bitstream decoding and manipulation. In the high quality video coding systems, high-performance bitstream decoding and manipulation is inevitable. However, there are certain factors influencing the improvement of the performance in the VLD process. One is that VLC codewords do not have any explicit word boundaries according to the VLC coding property. Thus, in the VLD process we do not know in advance the start of the next VLC until the previous VLC is decoded. Because of this phenomenon, the length of the decoded VLC codewords in the current cycle must be fed back for the next cycle to determine the start of next VLC. This induces that there is a feedback loop in the VLD process during two adjacent cycles, which limits the speed improvement of the VLD process.

On the other hand, four types of escape codes in the MPEG4 video coding systems would also slow down the VLD process. The escape codes in many video compression standards like MPEG1, MPEG2, H.26X, and MPEG4 are used as 2-D Huffman Code. The codewords that follow the escape code in MPEG-1, MPEG-2, H.261, and H.263 video coding standards are in fixed length. Hence, it is easy to handle the situation when escape occurs. However, the four types of escape code in MPEG-4 video coding standard makes it more difficult to design the high-performance VLD decoder.

In order to resolve the above-mentioned problems in improving the VLD performance, we propose a high-performance bitstream processing IP core for MPEG4 video coding system. The proposed IP core exploits the concurrent operations in the MPEG4 entropy decoding to achieve high performance in terms of limited hardware cost. The implementation results show that the proposed IP core operates at 125MHz clock frequency (i.e. 2000 Mbps) at the cost of 0.22 mm² silicon area based on a 0.25um CMOS technology. This performance achieves the real-time bit-stream processing requirement in the MPEG4 4CIF video decoding @30Hz. Besides, in order to facilitate the platform-based SOC design, the proposed IP core has been qualified through RTL coding check by NOVAS nLint following RMM coding rules [20] and RTL code coverage check by TRANSEDA VN-cover in terms of near 100% code coverage.

2. PREVIOUS WORKS
There have been various approaches presented to implement a VLD. The simplest and easiest way to implement a VLD is to decode the VLC data bit by bit [6]. However, this design is not suitable for high-quality compression system with high bit-rates, because it can only decode one bit per cycle. In contrary, the bit-parallel VLD design that can process more than one bit per cycle is more suitable for high-quality video compression systems. The